PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Dale E. Gulick	Customer No. 8012
Serial No.: 10/005,648	Examiner: Thomas J. Cleary
Filed: December 3, 2001	Group Art Unit: 2111
For: EMBEDDED PROCESSOR SUPPORTING BOTH ACPI AND ASF OPERATIONS	Att'y Docket: 2000.051600 Customer No. 26290

APPEAL BRIEF

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby submits this Appeal Brief to the Board of Patent Appeals and Interferences in response to the final Office Action dated September 20, 2006. A Notice of Appeal was filed on December 12, 2006 and so this Appeal Brief is believed to be timely filed.

The Commissioner is authorized to deduct the fee for filing this Appeal Brief ($500) from **Williams, Morgan & Amerson's P.C. Deposit Account 50-0786/2000.051600.**

I. REAL PARTY IN INTEREST

The present application is owned by Advanced Micro Devices, Inc. The assignment of the present application to Advanced Micro Devices, Inc., is recorded at Reel 12361, Frame 0071.

II. RELATED APPEALS AND INTERFERENCES

Applicant is not aware of any related appeals and/or interferences that might affect the outcome of this proceeding.

III. STATUS OF THE CLAIMS

Claims 1-85 are pending in the present application. However, claims 31-40, 51-54, 56-74, and 76-85 have been withdrawn from consideration in response to a restriction requirement imposed by the Examiner. Thus, claims 1-30, 41-50, 55, and 75 are the subject of this appeal.

Claims 1-5, 9-22, 30, and 41-50 stand rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Lindsay (U.S. Patent Application Publication No. 2002/0194415). Claims 6 and 23 stand rejected under 35 U.S.C. § 103(a) as allegedly being obvious over Lindsay in view of what was allegedly well-known in the art. Claims 7-8 and 24-26 stand rejected under 35 U.S.C. § 103(a) as allegedly being obvious over Lindsay in view of the admitted prior art. Claims 27-29 stand rejected under 35 U.S.C. § 103(a) as allegedly being obvious over Lindsay in view of Deschapper (U.S. Patent No. 6,199,134). Claims 55 and 75 stand rejected under 35 U.S.C. § 103(a) as allegedly being obvious over Lindsay, the admitted prior art, and Deschapper.

IV. STATUS OF AMENDMENTS

There were no amendments after the final rejections.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 sets forth a microcontroller that is configurable as either an Alert Standard Format master or an Alert Standard Format slave. The microcontroller is configured as either the Alert Standard Format master or the Alert Standard Format slave and the microcontroller is further configured as an Advanced Configuration and Power Interface controller. For example, Figure 4 shows one embodiment of the ASF south bridge 212 that includes a microcontroller MC 320 may be coupled to an SMBus 215. The processor (CPU) 202 and the microcontroller MC 320 can master the SMBus 215 or, when the ASF NIC 109 is present, the ASF south bridge 212 microcontroller MC 320 can operate in slave mode. The MC 320 may use software-driven I/O ports for the SMBus protocol, according to one aspect of the present invention, using so-called "chapter 13 interfaces" of the ACPI Specification, named from their definition given in chapter 13 of the ACPI Specification. See Patent Application, page 24, ll. 1-10.

Independent claim 9 sets forth an integrated circuit that includes an internal bus and a microcontroller connected to the internal bus. The microcontroller is configurable as either an Alert Standard Format master or an Alert Standard Format slave. The microcontroller is configured as either the Alert Standard Format master or the Alert Standard Format slave and the microcontroller is further configured as an Advanced Configuration and Power Interface controller. For example, Figure 4 shows one embodiment of the ASF south bridge 212 that may be formed as an integrated circuit. The ASF south bridge 212 includes a microcontroller MC 320 may be coupled to an SMBus 215. The processor (CPU) 202 and the microcontroller MC 320 can master the SMBus 215 or, when the ASF NIC 109 is present, the ASF south bridge 212

microcontroller MC 320 can operate in slave mode. The MC 320 may use software-driven I/O ports for the SMBus protocol, according to one aspect of the present invention, using so-called "chapter 13 interfaces" of the ACPI Specification, named from their definition given in chapter 13 of the ACPI Specification. See Patent Application, page 24, ll. 1-10.

Independent claim 41 sets forth an external bus, a processor coupled to the external bus, and an integrated circuit. The integrated circuit includes an internal bus, a bus interface logic connected to the external bus, and a microcontroller connected to the internal bus. The microcontroller is configurable as either an Alert Standard Format master or an Alert Standard Format slave. The microcontroller is configured as either the Alert Standard Format master or the Alert Standard Format slave and the microcontroller is further configured as an Advanced Configuration and Power Interface controller. For example, Figure 4 shows one embodiment of the ASF south bridge 212 that may be formed as an integrated circuit. The ASF south bridge 212 includes an internal south bridge bus 302 that couples a south bridge register 304 with an internal bus interface 338 of an Ethernet controller 344 and an LPC bridge 330. See Patent Application, page 23, ll. 6-13. The ASF south bridge 212 includes a microcontroller MC 320 may be coupled to an SMBus 215. The processor (CPU) 202 and the microcontroller MC 320 can master the SMBus 215 or, when the ASF NIC 109 is present, the ASF south bridge 212 microcontroller MC 320 can operate in slave mode. The MC 320 may use software-driven I/O ports for the SMBus protocol, according to one aspect of the present invention, using so-called "chapter 13 interfaces" of the ACPI Specification, named from their definition given in chapter 13 of the ACPI Specification. See Patent Application, page 24, ll. 1-10.

Independent claim 55 sets forth a method for operating a computer system. The method includes receiving an Alert Standard Format message at a microcontroller in the Alert Standard

Format south bridge and receiving an ACPI event notification at the microcontroller in the Alert Standard Format south bridge. Independent claim 55 also sets forth causing a system management interrupt to be generated using the microcontroller in the Alert Standard Format south bridge. For example, the MC 320 in the ASF south bridge 400 may receive an ASF message. The ASF south bridge 400 may also receive a plurality of ACPI event notifications at a plurality of ACPI interfaces 316A-316D to the MC 320 in the ASF south bridge 400, in step 810. A microcontroller interrupt may be generated to the MC 320 in the ASF south bridge 400. The microcontroller interrupt may be generated, for example, using the CPU-MC interrupt register 312. The MC 320 in the ASF south bridge 400 may then generate an SMI. The SMI may be generated using the SMI request register 306 in the ASF south bridge or the corresponding SMM initiator 325A or SMM initiation register 325B. See Patent Application, page 30, l. 12 – page 31, l. 4.

Independent claim 75 sets forth a south bridge. The south bridge includes a controller means for receiving an Alert Standard Format message, a controller means for receiving an ACPI event notification, and means for generating a system management interrupt. For example, the MC 320 in the ASF south bridge 400 may receive an ASF message. The ASF south bridge 400 may also receive a plurality of ACPI event notifications at a plurality of ACPI interfaces 316A-316D to the MC 320 in the ASF south bridge 400, in step 810. A microcontroller interrupt may be generated to the MC 320 in the ASF south bridge 400. The microcontroller interrupt may be generated, for example, using the CPU-MC interrupt register 312. The MC 320 in the ASF south bridge 400 may then generate an SMI. The SMI may be generated using the SMI request register 306 in the ASF south bridge or the corresponding SMM initiator 325A or SMM initiation register 325B. See Patent Application, page 30, l. 12 – page 31, l. 4.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Appellant respectfully requests that the Board review and overturn the rejections present in this case. The following issues are presented on appeal in this case:

(A) Whether claims 1-5, 9-22, 30, and 41-50 are anticipated by Lindsay

(B) Whether claims 6 and 23 are obvious over Lindsay in view of what was allegedly well-known in the art;

(C) Whether claims 7-8 and 24-26 are obvious over Lindsay in view of the admitted prior art;

(D) Whether claims 27-29 are obvious over Lindsay in view of Deschapper; and

(E) Whether claims 55 and 75 are obvious over Lindsay, the admitted prior art, and Deschapper.

VII. ARGUMENT

A. Legal Standards

An anticipating reference by definition must disclose every limitation of the rejected claim in the same relationship to one another as set forth in the claim. *In re Bond*, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990).

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference

teachings. That is, there must be something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561 (Fed. Cir. 1986). In fact, the absence of a suggestion to combine is dispositive in an obviousness determination. *Gambro Lundia AB v. Baxter Healthcare Corp.*, 110 F.3d 1573 (Fed. Cir. 1997). The mere fact that the prior art can be combined or modified does not make the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01. Third, there must be a reasonable expectation of success.

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142. A recent Federal Circuit case emphasizes that, in an obviousness situation, the prior art must disclose each and every element of the claimed invention, and that any motivation to combine or modify the prior art must be based upon a suggestion in the prior art. *In re Lee*, 61 U.S.P.Q.2d 143 (Fed. Cir. 2002). Conclusory statements regarding common knowledge and common sense are insufficient to support a finding of obviousness. *Id.* at 1434-35. Moreover, it is the claimed invention, as a whole, that must be considered for purposes of determining obviousness. A mere selection of various bits and pieces of the claimed invention from various sources of prior art does not render a claimed invention obvious, unless there is a suggestion or motivation in the prior art for the claimed invention, when considered as a whole.

B. Claims 1-5, 9-22, 30, and 41-50 are not anticipated by Lindsay.

Lindsay describes a controller 700 that is adapted to accommodate at least one protocol intended to effect management functionality. Aspects of such management functionality can be defined by the Alert Standard Format (ASF) specification protocol, the Advanced Configuration and Power Interface Specification protocol (ACPI), and other protocols. See Lindsay [0074-0075]. Lindsay also describes an alerting network controller that can be similar in functionality to controller 825, which is an alert supervisory bus controller that operates according to the Alert Standard Format. See Lindsay paragraphs [0083, 0086]. Lindsay also describes an ASF Configuration Application 922 that may retrieve data represented in an ASF Table via an Advanced Configuration and Power Interface (ACPI) mechanism. See Lindsay, paragraph [0096].

The Examiner then alleges that the components of controllers 700 and 825 operate according to the ACPI protocol and that the configuration application 922 uses the ACPI protocol for configuration. Although the controllers 700, 825 and the configuration application 922 may operate in accordance with the ACPI protocol, Applicants respectfully submit that none of these entities act as an ACPI controller. Applicants respectfully submit that persons of ordinary skill in the art will appreciate that an ACPI controller is a controller that is configured to implement various mechanisms defined by the ACPI protocol. The mechanisms defined by the ACPI protocol may be accessed or utilized by other entities within the computer system to perform operations in accordance with the ACPI protocol. For example, as described in Lindsay, the ASF Configuration Application 922 may retrieve data represented in an ASF Table via an ACPI mechanism. See Lindsay, paragraph [0096]. Although the ASF Configuration Application 922 may operate in accordance with the ACPI protocol, Applicant respectfully submits that it is not an ACPI controller.

Accordingly, Applicant respectfully submits that Lindsay fails to teach or suggest a microcontroller that is configured as either an Alert Standard Format master or slave and is further configured as an Advanced Configuration and Power Interface (ACPI) controller, as set forth in independent claims 1, 9, and 41. Applicant therefore submits that independent claims 1, 9, 41, and all claims depending therefrom, are not anticipated by Lindsay and requests that the Examiner's rejections of claims 1-5, 9-22, 30, and 41-50 under 35 U.S.C. § 102(e) be REVERSED.

C. Claims 6 and 23 are not obvious over Lindsay in view of what was allegedly well-known in the art.

Claims 6 and 23 depend from independent claims 1 and 9, respectively. As discussed above with regard to independent claims 1 and 9, Lindsay fails to teach or suggest a microcontroller that is configured as either an Alert Standard Format master or slave and is further configured as an Advanced Configuration and Power Interface (ACPI) controller. In rejecting claims 6 and 23, the Examiner takes Official Notice that embedded 8051 microcontrollers are well-known in the art. However, the Official Notice fails to remedy the fundamental deficiencies in the primary reference. Consequently, Applicant respectfully submits that the prior art of record fails to teach or suggest all the limitations of the claimed invention.

For at least the aforementioned reasons, Applicant respectfully submit that the Examiner has failed to make a *prima facie* case that the present invention is obvious over the prior art of record. Applicant requests that the Examiner's rejections of claims 6 and 23 under 35 U.S.C. § 103(a) be REVERSED.

D. Claims 7-8 and 24-26 are not obvious over Lindsay in view of the admitted prior art.

Claims 7-8 and 24-26 depend from independent claims 1 and 9, respectively. As discussed above with regard to independent claims 1 and 9, Lindsay fails to teach or suggest a microcontroller that is configured as either an Alert Standard Format master or slave and is further configured as an Advanced Configuration and Power Interface (ACPI) controller. The Examiner relies upon the background section of the present application to teach a microcontroller in a south bridge. However, the background section of the present application fails to remedy the fundamental deficiencies in the primary reference. Consequently, Applicant respectfully submits that the prior art of record fails to teach or suggest all the limitations of the claimed invention.

For at least the aforementioned reasons, Applicant respectfully submit that the Examiner has failed to make a *prima facie* case that the present invention is obvious over the prior art of record. Applicant requests that the Examiner's rejections of claims 7-8 and 24-26 under 35 U.S.C. § 103(a) be REVERSED.

E. Claims 27-29 are not obvious over Lindsay in view of Deschapper.

Claims 27-29 depend from independent claim 9. As discussed above with regard to independent claim 9, Lindsay fails to teach or suggest a microcontroller that is configured as either an Alert Standard Format master or slave and is further configured as an Advanced Configuration and Power Interface (ACPI) controller. The Examiner relies upon Deschepper to describe ACPI controller interfaces. However, Deschepper fails to remedy the fundamental

deficiencies in the primary reference. Consequently, Applicant respectfully submits that the prior art of record fails to teach or suggest all the limitations of the claimed invention.

For at least the aforementioned reasons, Applicant respectfully submit that the Examiner has failed to make a *prima facie* case that the present invention is obvious over the prior art of record. Applicant requests that the Examiner's rejections of claims 27-29 under 35 U.S.C. § 103(a) be REVERSED.

F. Claims 55 and 75 are not obvious over Lindsay, the admitted prior art, and Deschapper.

As discussed above, Lindsay fails to teach or suggest a microcontroller that is configured as either an Alert Standard Format master or slave and is further configured as an Advanced Configuration and Power Interface (ACPI) controller, as discussed above. Consequently, Applicant respectfully submits that Lindsay fails to teach or suggest receiving an Alert Standard Format message at a microcontroller in the Alert Standard Format south bridge and receiving an ACPI event notification at the microcontroller in the Alert Standard Format south bridge, as set forth in independent claims 55 and 75.

The Examiner relies upon the background section of the present application to teach a microcontroller in a south bridge and Deschepper to describe ACPI controller interfaces. However, none of these secondary references remedy the fundamental deficiencies in the primary reference. Consequently, Applicant respectfully submits that the prior art of record fails to teach or suggest all the limitations of the claimed invention.

For at least the aforementioned reasons, Applicant respectfully submit that the Examiner has failed to make a *prima facie* case that the present invention is obvious over the prior art of

record. Applicant requests that the Examiner's rejections of claims 55 and 75 under 35 U.S.C. § 103(a) be REVERSED.

VIII. CLAIMS APPENDIX

The claims that are the subject of the present appeal – claims 1-30, 41-50, 55, and 75 – are set forth in the attached "Claims Appendix."

IX. EVIDENCE APPENDIX

There is no separate Evidence Appendix for this appeal.

X. RELATED PROCEEDINGS APPENDIX

There is no Related Proceedings Appendix for this appeal.

XI. CONCLUSION

In view of the foregoing, it is respectfully submitted that the Examiner erred in not allowing all claims pending in the present application, claims 1-30, 41-50, 55, and 75, over the prior art of record. The undersigned may be contacted at (713) 934-4052 with respect to any questions, comments or suggestions relating to this appeal.

Respectfully submitted,

Date: February 12, 2007

/Mark W. Sincell/

Mark W. Sincell, Ph.D.
Reg. No. 52,226
WILLIAMS, MORGAN & AMERSON
10333 Richmond, Suite 1100
Houston, Texas 77042
(713) 934-7000
(713) 934-7011 (facsimile)

AGENT FOR APPLICANTS

CLAIMS APPENDIX

1. A microcontroller configurable as either an Alert Standard Format master or an Alert Standard Format slave, wherein the microcontroller is configured as either the Alert Standard Format master or the Alert Standard Format slave, wherein the microcontroller is further configured as an Advanced Configuration and Power Interface controller.

2. The microcontroller of claim 1, configured as the Alert Standard Format master.

3. The microcontroller of claim 2, wherein the microcontroller is coupled to an SMBus, and the microcontroller is further configured to receive Alert Standard Format status data from Alert Standard Format devices over the SMBus.

4. The microcontroller of claim 1, configured as the Alert Standard Format slave.

5. The microcontroller of claim 4, wherein the microcontroller is configured to receive status data from one or more Alert Standard Format devices, wherein the microcontroller is further configured to forward the status data from the one or more Alert Standard Format devices to the Alert Standard Format master.

6. The microcontroller of claim 1, further configured as an embedded 8051 microcontroller.

7. The microcontroller of claim 1, comprised in a bridge.

8. The microcontroller of claim 7, wherein the bridge is a south bridge.

9. An integrated circuit, comprising:

an internal bus; and

a microcontroller connected to the internal bus, wherein the microcontroller is configured to master the internal bus, wherein the microcontroller is configurable as either an Alert Standard Format (ASF) master or an ASF slave, wherein the microcontroller is configured as either the ASF master or the ASF slave, wherein the microcontroller is further configured as an Advanced Configuration and Power Interface (ACPI) controller.

10. The integrated circuit of claim 9, wherein the microcontroller is configured as the ASF master.

11. The integrated circuit of claim 10, wherein the microcontroller is coupled to an SMBus, wherein the microcontroller is further configured to receive ASF status data from one or more ASF devices over the SMBus.

12. The integrated circuit of claim 10, further comprising:

an Ethernet controller coupled to the internal bus, wherein the Ethernet controller and the microcontroller are configured to exchange data over the internal bus.

13. The integrated circuit of claim 12, further comprising:

a plurality of buffers coupled between the microcontroller and the Ethernet controller for buffering the data.

14. The integrated circuit of claim 13, wherein the plurality of buffers are connected between the internal bus and the Ethernet controller.

15. The integrated circuit of claim 12, and wherein the Ethernet controller is configured to route Alert Standard Format messages to the microcontroller.

16. The integrated circuit of claim 12, further comprising:

a remote management and control protocol set command unit connected to the internal bus, wherein the remote management and control protocol set command unit is configured to execute remote management and control protocol commands received from an external management server through the Ethernet controller.

17. The integrated circuit of claim 9, wherein the microcontroller is configured as the ASF slave.

18. The integrated circuit of claim 17, wherein the microcontroller is configured to receive status data from one or more ASF devices, wherein the microcontroller is further configured to forward the status data from the one or more ASF devices to a remote ASF master.

19. The integrated circuit of claim 17, further comprising:

an Ethernet controller coupled to the internal bus, wherein the Ethernet controller and the microcontroller are configured to exchange data over the internal bus.

20. The integrated circuit of claim 19, further comprising:

a plurality of buffers coupled between the microcontroller and the Ethernet controller for buffering the data.

21. The integrated circuit of claim 20, wherein the plurality of buffers are connected between the internal bus and the Ethernet controller.

22. The integrated circuit of claim 19, wherein the Ethernet controller is configured to route ASF messages to an external ASF master.

23. The integrated circuit of claim 9, wherein the microcontroller is further configured as an embedded 8051 microcontroller.

24. The integrated circuit of claim 9, wherein the integrated circuit is configured as a bridge, wherein the bridge further includes:

a first bus interface logic for coupling to a first external bus; and

a second bus interface logic for coupling to a second external bus.

25. The bridge of claim 24, wherein the bridge is configured as a south bridge.

26. The south bridge of claim 25, further comprising:

a plurality of south bridge registers; and

a register bridge connected to the internal bus, wherein the microcontroller is configured to read each of the plurality of south bridge registers through the register bride.

27. The integrated circuit of claim 9, further comprising:

a first ACPI embedded controller interface.

28. The integrated circuit of claim 27, further comprising:

a second ACPI embedded controller interface.

29. The integrated circuit of claim 28, further comprising:

a third ACPI embedded controller interface.

30. The integrated circuit of claim 9, further comprising:

an ASF status register.

31. An integrated circuit, comprising:

an internal bus;

a microcontroller connected to the internal bus, wherein the microcontroller is configured to master the internal bus, wherein the microcontroller is further configured as an Advanced Configuration and Power Interface (ACPI) controller; and

a plurality of ACPI embedded controller interfaces.

32. The integrated circuit of claim 31, wherein each of the plurality of ACPI embedded controller interfaces is configured as a private ACPI embedded controller interface.

33. The integrated circuit of claim 31, wherein the microcontroller is further configured as an embedded 8051 microcontroller.

34. The integrated circuit of claim 31, wherein the integrated circuit is configured as a bridge, wherein the bridge further includes:

a first bus interface logic for coupling to a first external bus; and

a second bus interface logic for coupling to a second external bus.

35. The bridge of claim 34, wherein the bridge is configured as a south bridge.

36. The south bridge of claim 35, further comprising:

a plurality of south bridge registers; and

a register bridge connected to the internal bus, wherein the microcontroller is configured to read each of the plurality of south bridge registers through the register bride.

37. An integrated circuit, comprising:

an internal bus;

a microcontroller connected to the internal bus, wherein the microcontroller is configured to master the internal bus, wherein the microcontroller is further configured as an Advanced Configuration and Power Interface (ACPI) controller;

an interrupt register configured to receive an entry from a processor, wherein an interrupt is generated to the microcontroller in response to the entry from the processor;

a data exchange register configured to receive one or more entries from the processor; and

one or more ACPI embedded controller interfaces.

38. The integrated circuit of claim 37, wherein the microcontroller is configured to write one or more entries in the data exchange register.

39. The integrated circuit of claim 37, wherein the microcontroller is configured to read the one or more entries in the data exchange register.

40. The integrated circuit of claim 37, wherein each of the one or more ACPI embedded controller interfaces is configured as a private ACPI embedded controller interface.

41. A computer system, comprising:

an external bus;

an integrated circuit, comprising:

an internal bus;

a microcontroller connected to the internal bus, wherein the microcontroller is configured to master the internal bus, wherein the microcontroller is configurable as either an

Alert Standard Format (ASF) master or an ASF slave, wherein the microcontroller is configured as either the ASF master or the ASF slave, wherein the microcontroller is further configured as an Advanced Configuration and Power Interface (ACPI) controller; and

a bus interface logic connected to the external bus; and

a processor coupled to the external bus.

42. The computer system of claim 41, wherein the microcontroller is configured as the ASF master for the computer system.

43. The computer system of claim 42, further comprising:

an SMBus;

one or more ASF devices coupled to the SMBus; and

wherein the microcontroller is further configured to receive ASF status data from the one or more ASF devices over the SMBus.

44. The computer system of claim 42, further comprising:

an Ethernet controller coupled to the internal bus, wherein the Ethernet controller and the microcontroller are configured to exchange data over the internal bus; and

wherein the processor is configured to communicate over a network using the Ethernet controller.

45. The computer system of claim 44, and wherein the Ethernet controller is configured to route Alert Standard Format messages to the microcontroller.

46. The computer system of claim 44, further comprising:

a remote management and control protocol set command unit connected to the internal bus, wherein the remote management and control protocol set command unit is configured to execute remote management and control protocol commands received from an external management server through the Ethernet controller.

47. The computer system of claim 41, wherein the microcontroller is configured as the ASF slave.

48. The computer system of claim 47, wherein the microcontroller is configured to receive status data from one or more ASF devices, wherein the microcontroller is further configured to forward the status data from the one or more ASF devices to a remote ASF master.

49. The computer system of claim 48, further comprising:

a network interface card coupled to the integrated circuit and to the processor, wherein the network interface card is configured as the Alert Standard Format master, and wherein the Ethernet controller is configured to route Alert Standard Format messages to the network interface card.

50. The computer system of claim 47, further comprising:

an Ethernet controller coupled to the internal bus, wherein the Ethernet controller and the microcontroller are configured to exchange data over the internal bus.

51. A computer system, comprising:

an external bus;

an integrated circuit, comprising:

an internal bus;

a microcontroller connected to the internal bus, wherein the microcontroller is configured to master the internal bus, wherein the microcontroller is further configured as an Advanced Configuration and Power Interface (ACPI) controller;

a plurality of ACPI embedded controller interfaces; and

a bus interface logic connected to the external bus; and

a processor coupled to the external bus.

52. The computer system of claim 51, wherein each of the plurality of ACPI embedded controller interfaces is configured as a private ACPI embedded controller interface.

53. A computer system, comprising:

an external bus;

a processor coupled to the external bus; and

an integrated circuit, comprising:

an internal bus;

a microcontroller connected to the internal bus, wherein the microcontroller is configured to master the internal bus, wherein the microcontroller is further configured as an Advanced Configuration and Power Interface (ACPI) controller;

an interrupt register configured to receive an entry from the processor, wherein an interrupt is generated to the microcontroller in response to the entry from the processor;

a data exchange register configured to receive one or more entries from the processor;

one or more ACPI embedded controller interfaces; and

a bus interface logic connected to the external bus.

54. The computer system of claim 53, wherein each of the plurality of ACPI embedded controller interfaces is configured as a private ACPI embedded controller interface.

55. A method for operating a computer system, the method comprising:

receiving an Alert Standard Format message at a microcontroller in the Alert Standard Format south bridge;

receiving an ACPI event notification at the microcontroller in the Alert Standard Format south bridge; and

causing a system management interrupt to be generated using the microcontroller in the Alert Standard Format south bridge.

56. A method for operating a computer system, the method comprising:

receiving a first ACPI event notification at a first ACPI interface to a microcontroller in a south bridge; and

receiving a second ACPI event notification at a second ACPI interface to the microcontroller in the south bridge.

57. The method of claim 56, wherein receiving the second ACPI event notification at the second ACPI interface to the microcontroller in the south bridge comprises receiving the second ACPI event notification at the second ACPI interface to the microcontroller in the south bridge concurrently with receiving the first ACPI event notification at the first ACPI interface to the microcontroller in the south bridge.

58. The method of claim 56, further comprising:

receiving a third ACPI event notification at a third ACPI interface to the microcontroller in the south bridge.

59. The method of claim 58, wherein receiving the second ACPI event notification at the second ACPI interface to the microcontroller in the south bridge comprises receiving the second ACPI event notification at the second ACPI interface to the microcontroller in the south bridge concurrently with receiving the first ACPI event notification at the first ACPI interface to the microcontroller in the south bridge.

60. The method of claim 59, wherein receiving the third ACPI event notification at the third ACPI interface to the microcontroller in the south bridge comprises receiving the third

ACPI event notification at the third ACPI interface to the microcontroller in the south bridge concurrently with receiving the first ACPI event notification at the first ACPI interface to the microcontroller in the south bridge.

61. The method of claim 57, further comprising:

receiving a fourth ACPI event notification at a fourth ACPI interface to the microcontroller in the south bridge.

62. The method of claim 57, further comprising:

causing a system management interrupt to be generated using the microcontroller in the south bridge.

63. A method for operating a computer system, the method comprising:

receiving an ACPI event notification at the microcontroller in the south bridge;

receiving one or more data entries in a data exchange register in the south bridge;

generating a microcontroller interrupt to the microcontroller in the south bridge; and

causing a system management interrupt to be generated using the microcontroller in the south bridge.

64. The method of claim 63, wherein generating the microcontroller interrupt to the microcontroller in the south bridge comprises generating the microcontroller interrupt to the microcontroller in the south bridge in response to receiving the one or more data entries in the data exchange register in the south bridge.

65. A computer readable medium encoded with instructions that, when executed by a computer system, performs a method for operating the computer system, the method comprising:

receiving an Alert Standard Format message at a microcontroller in the Alert Standard Format south bridge;

receiving an ACPI event notification at the microcontroller in the Alert Standard Format south bridge; and

causing a system management interrupt to be generated using the microcontroller in the Alert Standard Format south bridge.

66. A computer readable medium encoded with instructions that, when executed by a computer system, performs a method for operating the computer system, the method comprising:

receiving a first ACPI event notification at a first ACPI interface to a microcontroller in a south bridge; and

receiving a second ACPI event notification at a second ACPI interface to the microcontroller in the south bridge.

67. The computer readable medium of claim 66, wherein receiving the second ACPI event notification at the second ACPI interface to the microcontroller in the south bridge comprises receiving the second ACPI event notification at the second ACPI interface to

the microcontroller in the south bridge concurrently with receiving the first ACPI event notification at the first ACPI interface to the microcontroller in the south bridge.

68. The computer readable medium of claim 66, the method further comprising:

receiving a third ACPI event notification at a third ACPI interface to the microcontroller in the south bridge.

69. The computer readable medium of claim 68, wherein receiving the second ACPI event notification at the second ACPI interface to the microcontroller in the south bridge comprises receiving the second ACPI event notification at the second ACPI interface to the microcontroller in the south bridge concurrently with receiving the first ACPI event notification at the first ACPI interface to the microcontroller in the south bridge.

70. The computer readable medium of claim 69, wherein receiving the third ACPI event notification at the third ACPI interface to the microcontroller in the south bridge comprises receiving the third ACPI event notification at the third ACPI interface to the microcontroller in the south bridge concurrently with receiving the first ACPI event notification at the first ACPI interface to the microcontroller in the south bridge.

71. The computer readable medium of claim 67, the method further comprising:

receiving a fourth ACPI event notification at a fourth ACPI interface to the microcontroller in the south bridge.

72. The computer readable medium of claim 66, the method further comprising:

causing a system management interrupt to be generated using the microcontroller in the south bridge.

73. A computer readable medium encoded with instructions that, when executed by a computer system, performs a method for operating the computer system, the method comprising:

receiving an ACPI event notification at the microcontroller in the south bridge;

receiving one or more data entries in a data exchange register in the south bridge;

generating a microcontroller interrupt to the microcontroller in the south bridge; and

causing a system management interrupt to be generated using the microcontroller in the south bridge.

74. The computer readable medium of claim 73, wherein generating the microcontroller interrupt to the microcontroller in the south bridge comprises generating the microcontroller interrupt to the microcontroller in the south bridge in response to receiving the one or more data entries in the data exchange register in the south bridge.

75. A south bridge, comprising:

controller means for receiving an Alert Standard Format message;

controller means for receiving an ACPI event notification; and

means for generating a system management interrupt.

76. A south bridge, comprising:

first interface means for receiving a first ACPI event notification; and

second interface means for receiving a second ACPI event notification.

77. The south bridge of claim 76, wherein the first interface means and the second interface means operate concurrently.

78. The south bridge of claim 76, further comprising:

third interface means for receiving a third ACPI event notification.

79. The south bridge of claim 78, wherein the first interface means and the third interface means operate concurrently.

80. The south bridge of claim 79, wherein the second interface means and the third interface means operate concurrently.

81. The south bridge of claim 76, further comprising:

fourth interface means for receiving a fourth ACPI event notification.

82. The south bridge of claim 76, further comprising:

means for generating a system management interrupt.

83. A south bridge, comprising:

controller means for receiving an ACPI event notification;

means for receiving one or more data entries in a data exchange register;

means for generating an interrupt to the controller means for receiving an ACPI event notification; and

means for generating a system management interrupt.

84. A bridge, comprising:

an internal bus configured to transfer data in the bridge; and

a microcontroller coupled to transmit data over the internal bus.

85. The bridge of claim 84, wherein the bridge is a south bridge.